3.3V 10.7Gbps CML LIMITING POST AMPLIFIER W/ TTL SD AND /SD

SY88953L

FEATURES

- **Single 3.3V power supply**
- **Up to 10.7Gbps operation**
- **800mVp-p output swing with 30ps edge rates**
- **28dB voltage gain with 5mVp-p input sensitivity**
- **On chip 50Ω I/O termination**
- **Programmable signal detect (SD and /SD) with 6dB hysteresis**
- **Chatter-free OC-TTL SD and /SD outputs with internal 5kΩ pull-up resistors can feedback to TTL enable (/EN) input**
- **Available in a tiny (3mm × 3mm) 16-pin MLF® package or die**

APPLICATIONS

- **OC-192 SDH/SONET**
- **10G Ethernet/Fibre Channel receivers**
- **Upto 10.7Gbps proprietary link**
- **XFP transceivers**
- **Line driver/receiver**

DESCRIPTION

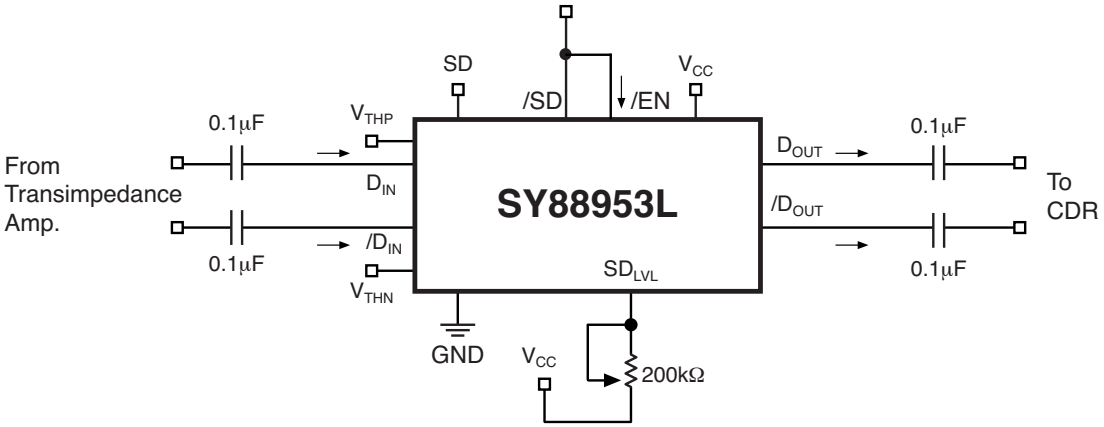
The SY88953L high-speed limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88953L quantizes these signals and outputs CML level waveforms.

The SY88953L operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 10.7Gbps and as small as 5mVp-p can be amplified to drive devices with CML inputs.

The SY88953L outputs TTL signal-detect (SD and /SD) signals. A programmable signal-detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. /SD is the complementary output of SD. /SD can be fedback to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN deasserts the true output signal without removing the input signal. Typically 6dB SD hysteresis is provided to prevent chattering.

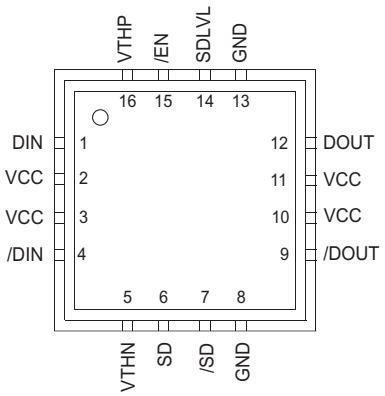
The SY88953L also includes an input threshold adjustment to correct pulsewidth distortion.

TYPICAL APPLICATIONS CIRCUIT



*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF®

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88953LMI	MLF-16	Industrial	953L	Sn-Pb
SY88953LMITR[1]	MLF-16	Industrial	953L	Sn-Pb
SY88953LMG	MLF-16	Industrial	953L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY88953LMGTR[1]	MLF-16	Industrial	953L with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1	DIN	Data Input	True data input w/50Ω resistor to V_{CC}.
2, 3, 10, 11	VCC	Power Supply	Positive power supply.
4	/DIN	Data Input	Complementary data input w/50Ω resistor to V_{CC}.
5	VTHN	Input	/DIN DC threshold adjustment pin.
6	SD	Open-collector TTL output w/ internal 5kΩ pull-up resistor	Signal-Detect: Asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
7	/SD	Open-collector TTL output w/ internal 5kΩ pull-up resistor	Inverted Signal-Detect: Asserts low when the data input amplitude rises above the threshold set by SD_{LVL}.
8, 13, EP	GND	Ground	Device ground. Exposed pad must be soldered to PCB ground for proper electrical and thermal performance.
9	/DOUT	CML Output	Complementary data output.
12	DOUT	CML Output	True data output.
14	SDLVL	Input	Signal-Detect Level Set: A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which SD will be asserted.
15	/EN	TTL Input: Default is high.	Enable: Deasserts true data output when high.
16	VTHP	Input	DIN DC threshold adjustement pin.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +4.0V
Data Input Voltage (D_{IN}, /D_{IN}) ... (V_{CC}–1.0V) to (V_{CC}+0.5V)
Data Output Voltage (D_{OUT}, /D_{OUT}) .....
..... (V_{CC}–1.0V) to (V_{CC}+0.5V)
Data Output Current ($D_{OUT,}$ /D_{OUT}) 22mA
/EN Voltage ..... 0 to V_{CC}
SD, /SD Current 5mA
SDLVL Voltage ..... (V_{CC}–1.3V) to V_{CC}
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Package Thermal Resistance[3]
MLF®
(θ_{JA}) Still-Air ..... 59°C/W
(ψ_{JB}) Still-Air ..... 32°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	no output load		110	170	mA
V_{SDLVL}	SDLVL Voltage		V_{CC}–1.3		V_{CC}	V
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = V_{CC}			20	µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA
V_{OH}	SD, /SD Output HIGH Level		2.4			V
V_{OL}	SD, /SD Output LOW Level	I_{OL} = +2mA			0.5	V
V_{OH}	Output HIGH Voltage	50Ω to V_{CC} output load	V_{CC}–0.020	V_{CC}–0.005	V_{CC}	V
V_{OL}	Output LOW Voltage	50Ω to V_{CC} output load	V_{CC}–0.560	V_{CC}–0.400	V_{CC}–0.240	V
V_{OFFSET}	Differential Output Offset				±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω
Z_O	Single-Ended Input Impedance		40	50	60	Ω

Note s:

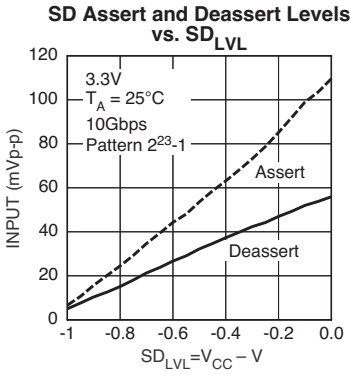
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Exposed pad must be soldrered to PCB's ground plane.

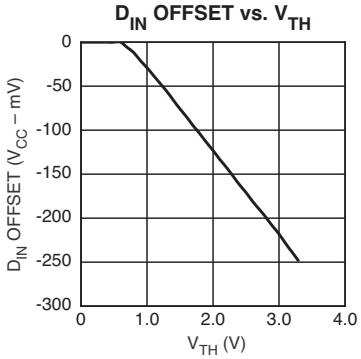
AC ELECTRICAL CHARACTERISTICS

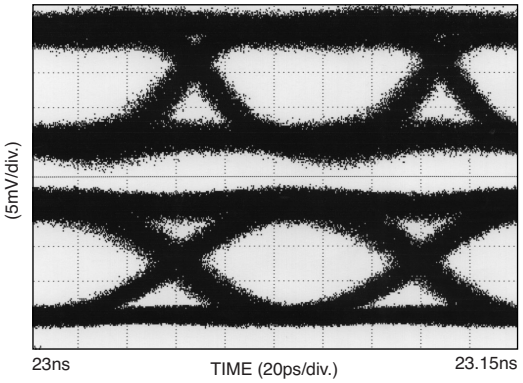
V_{CC} = 3.0V to 3.6V; R_{LOAD} = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
HYS	SD Hysteresis	electrical signal	2	6	8	dB
PSRR	Power Supply Rejection Ratio			35		dB
t_{OFF}	SD, /SD Release Time			0.1	0.5	µs
t_{ON}	SD, /SD Assert Time			0.2	0.5	µs
t_r,t_f	Output Rise/Fall Time	$V_{ID} \geq 50mV_{PP}$		30	35	ps
V_{ID}	Differential Input Voltage Swing		5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing		480	800	1120	mV_{PP}
V_{SR}	SD Sensitivity Range		5		50	mV_{PP}
$A_{V(Diff)}$	Differential Voltage Gain		22	28		dB
S_{21}	Single-Ended Small-Signal Gain		16	22		dB
B_{-3dB}	3dB Bandwidth			7.5		GHz

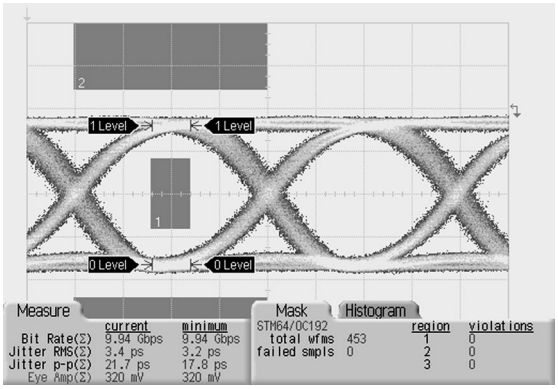
TYPICAL OPERATING CHARACTERISTICS







Example of Using V_{TH} to Cancel Effect of Pulse Width Distortion



(3.3V, 27°C, 10Gbps) $30mV_{PP}$ Differential Input

DETAILED DESCRIPTION

The SY88953L high-speed limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 10.7Gbps and as small as 5mVp-p can be amplified. Figure 1 shows the allowed input voltage swing. The SY88953L generates SD and /SD outputs. SD_{LVL} sets the sensitivity of the input amplitude detection. The SY88953L also includes an input threshold adjustment to correct pulsewidth distortion

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88953L's input stage. The high-sensitivity of the input amplifier allows signals as small as 5mVp-p to be detected and amplified. The input amplifier allows input signals as large as 1800mVp-p. Input signals are linearly amplified with a typically 28dB differential voltage gain. Since it is a limiting amplifier, the SY88953L outputs typically $800mV_{PP}$ voltage-limited waveforms for input signals that are greater than 32mVp-p. Applications requiring the SY88953L to operate with high-gain should have the upstream TIA placed as close as possible to the SY88953L's input pins to ensure the best performance of the device.

Threshold Adjustment

The SY88953L's duty cycle can be controlled by forcing an offset at either input using V_{THP} or V_{THN}. Typically, only one of the inputs is required to be adjusted, depending on the required direction of the pulse width adjustment. The SY88953L implements current source based offset control of the inputs. "Typical Operating Characteristics" shows the offset applied to the input for a given V_{TH} voltage. This feature is disabled by simply setting V_{TH} to GND.

Output Buffer

The SY88953L's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically 800mVp-p waveforms across 25Ω total loads. The output buffer thus switches typically 16mA tail-current.

Signal-Detect

The SY88953L generates chatter-free signal-detect (SD and /SD) open-collector TTL outputs with internal 5kΩ pullup resistors as shown in Figure 4. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. /SD is the complementary output of SD. /SD asserts low if the input amplitude rises above the threshold set by SD_{LVL} and deasserts high otherwise. /SD can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN deasserts the true output signal without removing the input signals. Typically 6dB SD hysteresis is provided to prevent chattering.

Signal-Detect Level Set

A programmable signal-detect level set pin (SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and SD_{LVL} sets the voltage at SD_{LVL}. This voltages ranges from V_{CC} to V_{CC}-1.3V. The external resistor creates a voltage divider between V_{CC} and V_{CC}-1.3V as shown in Figure 5. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from SD_{LVL} to V_{CC}, the smaller the SD sensitivity. Hence, larger input amplitude is required to assert SD. "Typical Operating Characteristics" shows the relationship between the input amplitude detection sensitivity and the SD_{LVL} voltage.

Hysteresis

The SY88953L provides typically 6dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log(power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence the same ratio can be stated as 20log(voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88953L provides typically 3dB SD optical hysteresis. As the SY88953L is an electrical device, this datasheet refers to hysteresis in electrical terms. With 6dB SD hysteresis, a voltage factor of two is required to assert or deassert SD.

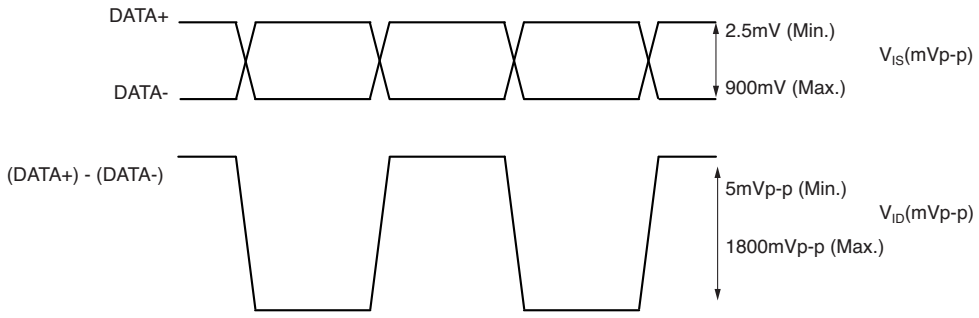


Figure 1. V_{IS} and V_{ID} Definitions

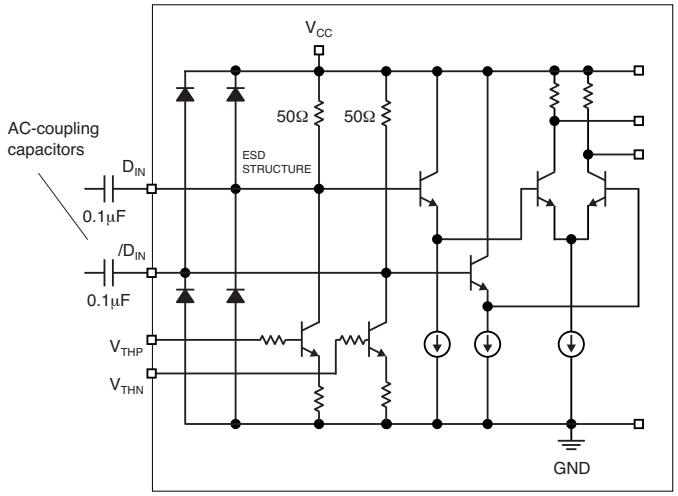


Figure 2. Input Structure

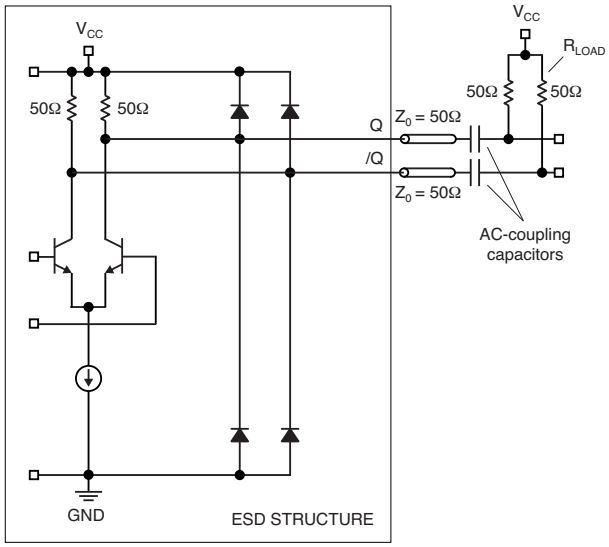


Figure 3. Output Structure

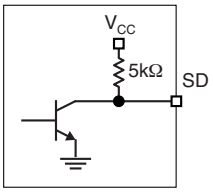


Figure 4. SD, /SD Output Structure

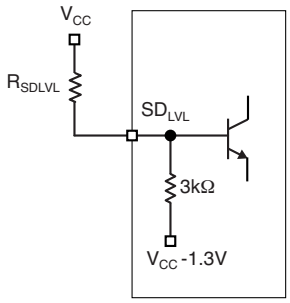
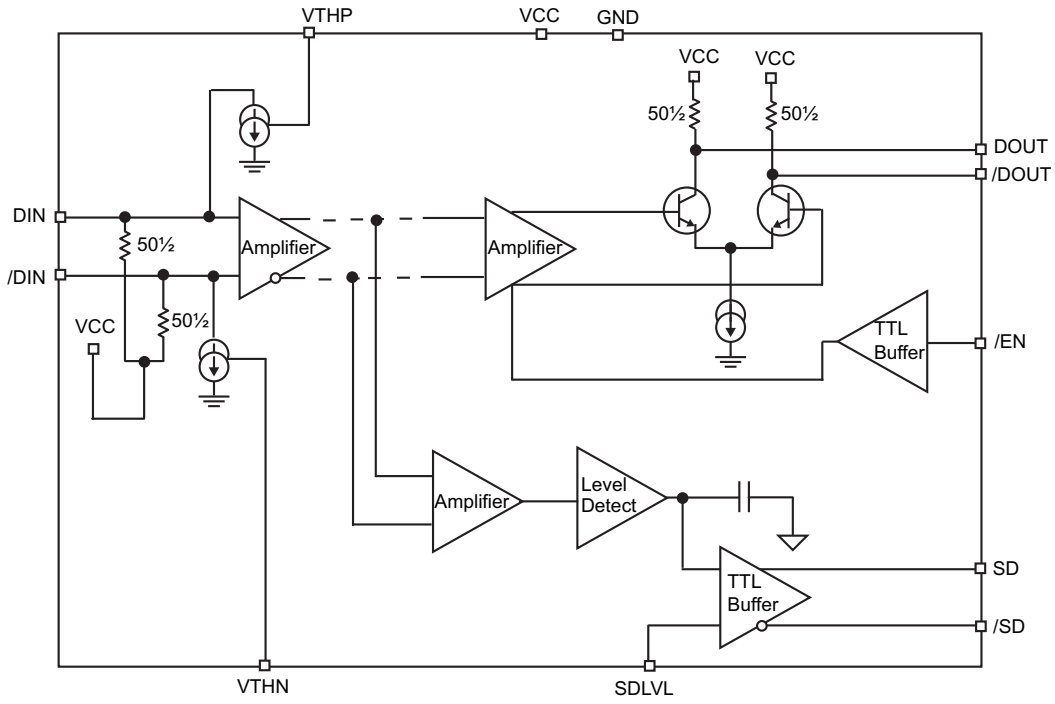


Figure 5. SD_{LVL} Setting Circuit

FUNCTIONAL BLOCK DIAGRAM



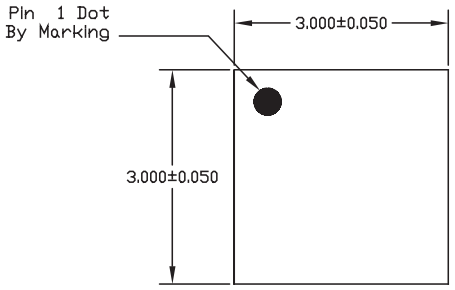
DESIGN PROCEDURE

Layout and PCB Design

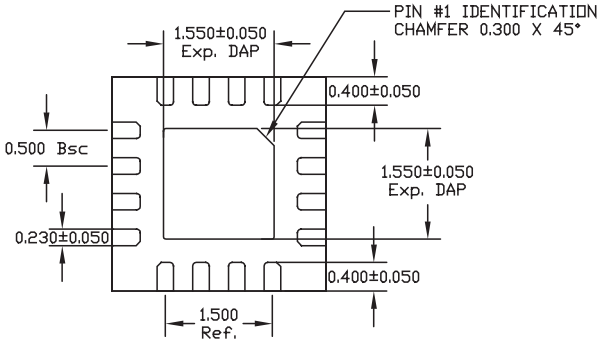
Since the SY88953L is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88953L's ground pins should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

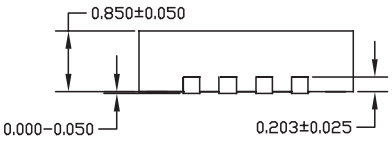
16-PIN MicroLeadFrame® (MLF-16)



TOP VIEW

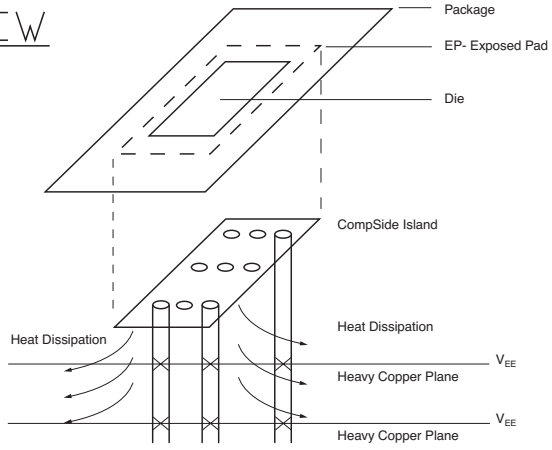


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are 100% baked and dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com